	Symbol	Conditions	Value	
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	39	
Drain to Source Voltage				V
			±20	
		L=0.4mH, T_C=25℃	45	
Power Dissipation	P_D	T_C=25℃		
Operating and Storage Temperature	T_J, T			℃

		Unit
Thermal Resistance Junction-Case	50	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	2	3	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=100V, T_j=25℃	-	-	1	A
		V_{GS}=0V, V_{DS}=100V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=15A	-	16.2	19	m
Transconductance	g_{fs}	V_{DS}=5V, I_D=10A	-	22	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.8	-	

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	716	-	pF
Output Capacitance	C_{oss}		-	146	-	
Reverse Transfer Capacitance	C_{rss}		-	4.4	-	
Total Gate Charge	Q_g(10V)	V_{DD}=50V, I_D=15A, V_{GS}=10V	-	13	-	nC
Gate to Source Charge	Q_{gs}		-	3.5	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=15A, V_{GS}=10V, R_G=10 ,	-	6	-	ns
Rise time	t_r		-	3	-	
Turn off Delay Time	$t_{d(off)}$		-	12	-	
Fall Time	t_f		-	3	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=15A, dI_F/dt=500A/ s	-	40	-	ns
Reverse Recovery Charge	Q_{rr}		-	150	-	nC

Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

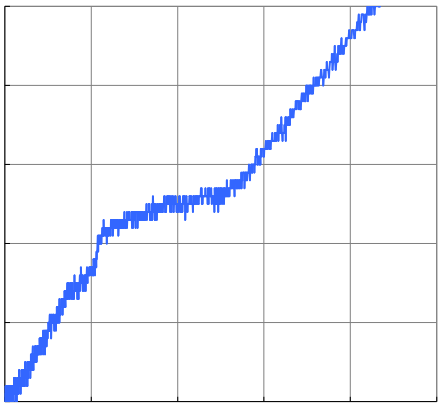
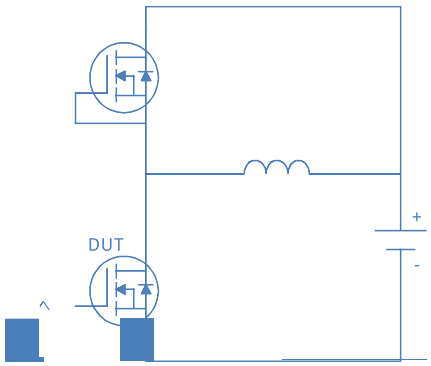
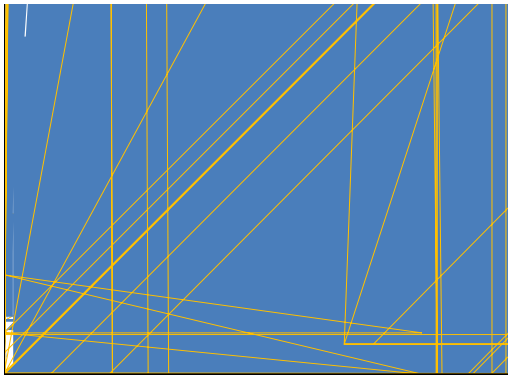
Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage
	

Figure 9. Maximum Safe Operating Area	Figure 10. Maximun Drain Current vs. Case Temperature

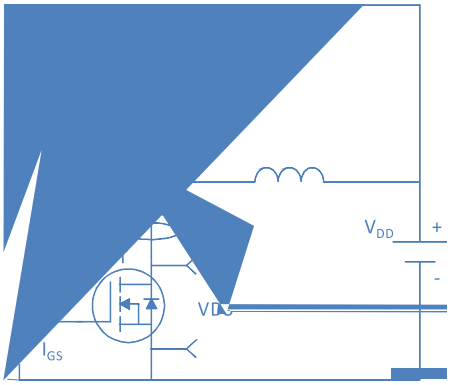
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

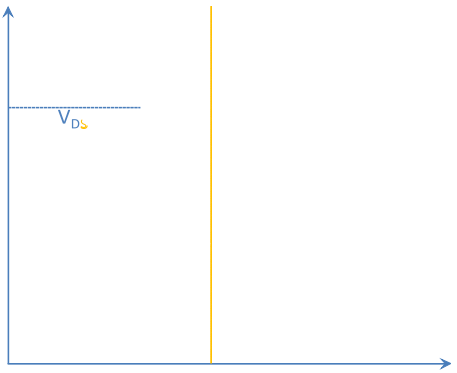
Inductive switching Test



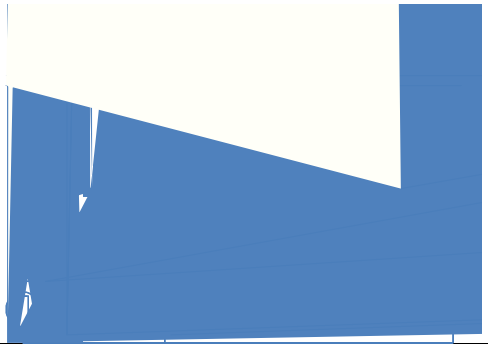


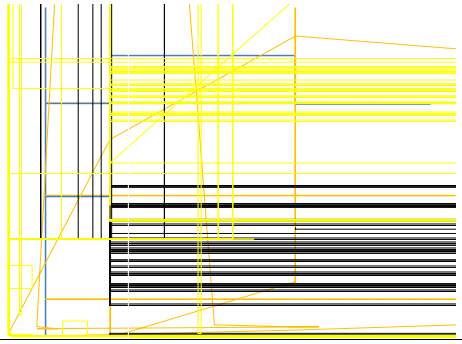
Gate Charge Test



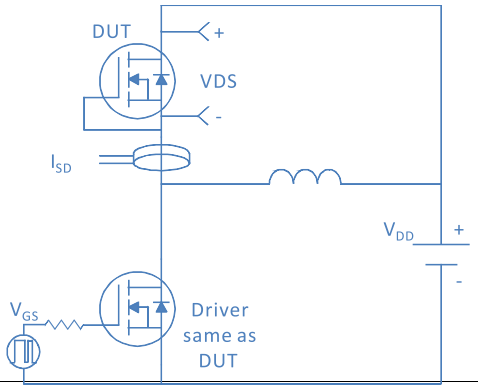


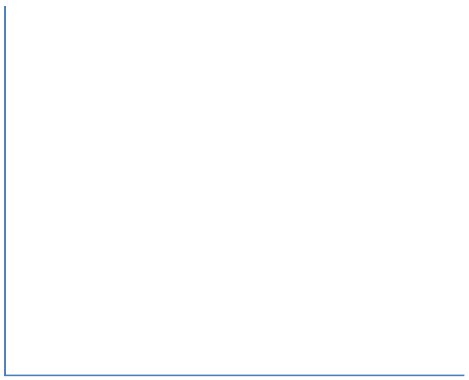
Uclamped Inductive Switching (UIS) Test





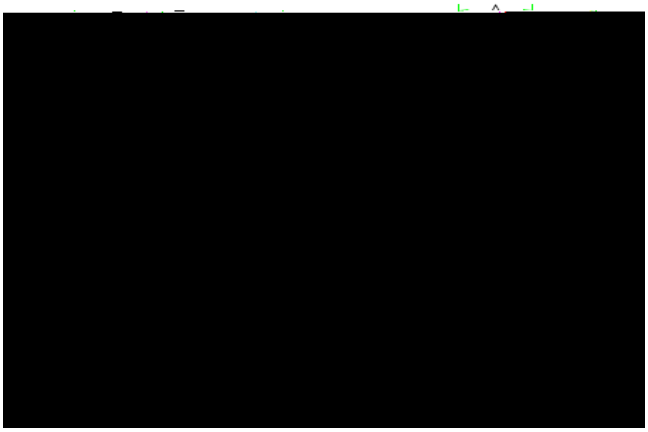
Diode Recovery Test



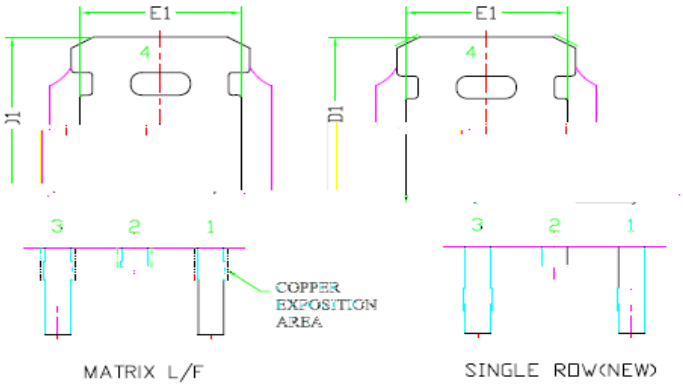


Package Outline

TO-252, 2 leads

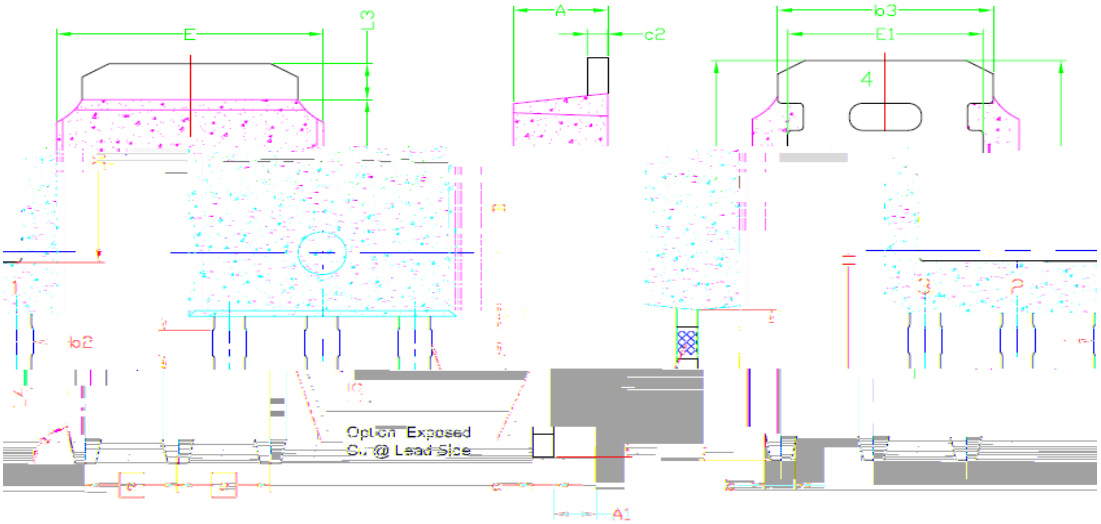


SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1		2.743 REF	
L2		0.508 BSC	
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223



Package Outline

TO-251, 3leads



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	3.98	4.13	4.28
L3	0.89	--	1.27
L4		0.698 REF	
L5	0.972	1.099	1.226
D	6.00	6.10	6.223
H	11.05	11.25	11.45
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e		2.286 BSC	
A	2.20	2.30	2.38
A1	0.89	1.04	1.15
c	0.46	0.50	0.60
c2	0.46	0.50	0.60
D1	5.10	--	--
E1	4.40	--	--
α		79° REF	